

Electrical Transportation Behavior of Magnetron Sputtered Al-Fe-Sn Thin Film

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Abstract: During the manufacturing process of Al-based thin films for electronic applications, a post-deposition annealing is required in order to achieve lower resistivity. However, the electrical transportation behavior of the magnetron sputtered Al film has been rarely investigated so far. To approach this objective, we have explored the microstructures of the films before and after annealing with emphasis on the structural features related to diffusion and interface using TEM observation. Hall-effect measurement was employed to determine the variation of carrier density and mobility brought by the evolution originating at the interface. The results demonstrate that during annealing an intimate contact is formed between the film and the substrate via diffusion, leading to a combination of high mobility and high density of the carriers. A model was proposed from the aspect of energy bands in order to explain the positive effect of the interfacial phenomenon upon electron conductivity.

Key words: electrical resistivity; Al-based thin film; electrical transportation

Al and Al alloy films with high characteristics are still now the major conductive materials in practical applications for many kinds of electrical equipments and power systems. The representative Al films as wires have been widely used for VLSI (very large scale integrations)^[1-3] and the buffer layer in ULSI (ultra large scale integrations)^[4-7]. Therefore, it is highly desirable to obtain Al films with low electrical resistivity, which is relatively difficult for several reasons. Firstly, the transportation of electrons is prohibited by the elastic scattering brought by external surface and grain boundaries contained in the films. The effect of external surface on electrical resistivity results in negative thickness dependence of the resistivity. In addition, variety of alloying elements needed to be added so that the formation of surface hillocks was avoided during film growth process^[8-15]. Unfortunately, the addition of alloying elements makes the transportation of charge carriers more difficult since the interference from lattice vibration became more severe.

In order to minimize the contribution of grain boundary scattering to resistivity, it is necessary to obtain the films composed of relatively coarse grains. Also, alloying elements

added could be dissolved from Al matrix so that the lattice distortion is diminished. Both of the purposes could be achieved via an annealing process of the film after deposition. It has been reported that the electrical resistivity as low as $\sim 5 \mu\Omega\cdot\text{cm}$ could be achieved via post-deposition annealing^[16,17]. The effect of post-deposition annealing on structural evolution and electrical resistivity has been investigated comprehensively^[18,19]. Previous results suggested that an optimized structure could actually lead to a much lower resistivity of the film via proper heat treatments.

Theoretically, the improved electrical conductivity should be attributed to the variation of charge carrier behavior. However, few works have been done on this aspect. In the present work, the electrical conductivity improvement of the Al-deposited film after annealing was explained based on Hall-effect measurement results. It was shown that the annealing introduced a combination of high density and mobility of charge carriers. We have proposed that such a combination should be attributed to the formation of the intimate contact between the film and the substrate, which led to a sheet resistivity even lower than that of the bulk materials.

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To prove the new mechanism, an energy band- related model was established to help explain the contribution from interfacial variation.

1 Experiment

0.725 μm thick Si(100) wafer ultrasonically cleaned by acetone, methanol and pure water in sequence was chosen as the substrate for magnetron sputtering deposition. Although SiO_2 or glass is widely used as the substrate for deposition due to their fully isolating nature^[20,21], for GLSI applications in which Al film is used as buffer layer, it is required to deposit the film directly on Si wafer. The target for deposition was manufactured mainly via powder metallurgy process. Two holes were symmetrically drilled along the diameter of a $\Phi 60$ mm Al-Sn alloy plate, in which two pure Fe columns were inserted. The ambient pressure in the system was retained to at 8×10^{-5} Pa before the deposition. The deposition process was performed under argon atmosphere (0.5 Pa) under an operating power of 30 W, and the deposition rate was $0.36 \text{ nm}\cdot\text{s}^{-1}$. Veeco DEKTAK Profilometer was employed to measure the mean thickness of the as-deposited film. The deposited film was then annealed under an gas pressure lower than 1×10^{-3} Pa at 823 K for 1 h.

The chemical composition of the as-deposited film was determined via inductively coupled plasma atomic emission spectrometry (ICP-AES) by the Shimatsu ICPE-9820 instrument. The chemical composition of the as-deposited alloy film was Fe 4.88 wt%; Sn 3.66 wt%; Al balance. The microstructures of the cross sections were observed by JEOL

JEM-2100 transmission electron microscope (TEM) equipped with energy dispersive spectrum (EDS). The electrical resistivity of the film was measured via a four-probe method. The mobility and the density of electrical carries in the film were determined by Hall-effect measurements at various temperatures ($T_s=4, 100, 200, 300$ K) in a magnetic field of 1.5 T.

2 Results and Discussion

2.1 Film microstructure

The microstructure of the as-deposited film is illustrated in Fig.1a. The film consists of grains with tens of nanometer in size. The high-resolution mode image shows the presence of native oxide at the interface between the silicon wafer and film (Fig.1b). The electronic diffraction pattern of the film (the inset graph in Fig.1b) shows that the film completely consists of α -Al phase. An observable structure transformation occurs during annealing process (Fig.1c and 1d). The grains in the film become hundreds of nanometers in planar direction. Although a single crystal type electronic diffraction pattern is obtained by masking a single grain, the polycrystalline structure is still maintained. In addition, a three-layer structure is present at the interfacial region between the annealed film and the substrate (Fig.1d). EDX was employed to determine the chemical composition of each of these three layers, whose results are listed in Table 1. It can be seen that the Al atoms in the film and Si atoms in the substrate mutually diffuse into each other, while the diffusion of alloying elements is not observed. The doping of Si substrate via Al diffusion results

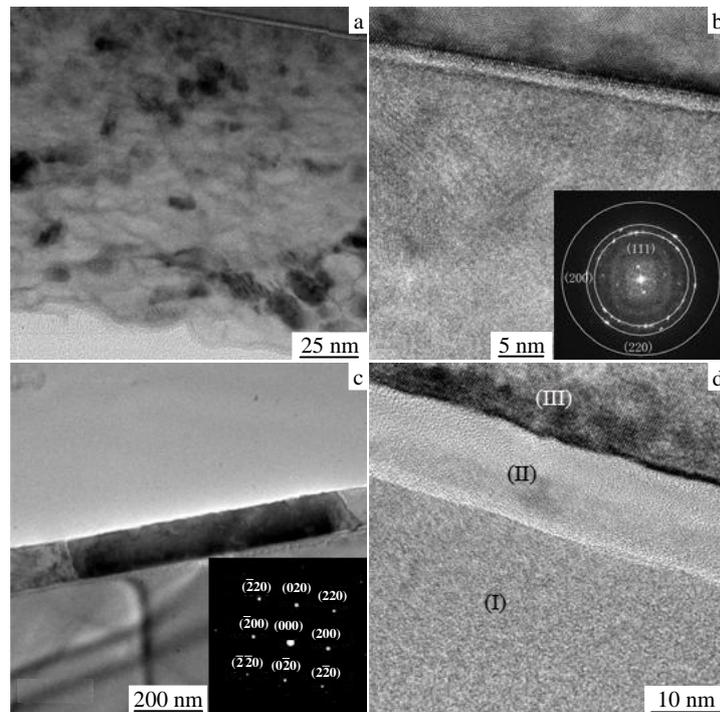


Fig.1 TEM microstructures and SEDP of as-deposit film (a, b) and 823 K annealed sample (c, d); (b, d) the high-resolution modes

Table 1 Compositions of three layers formed at the film-substrate interface regions as labeled in Fig.1d

Region	Al		Fe		Si		O	
	wt%	at%	wt%	at%	wt%	at%	wt%	at%
Layer (I)	64.16	70.13	18.37	9.63	15.36	16.11	2.25	4.13
Layer (II)	4.8	5.1	—	—	91.5	88.8	3.7	6.2
Layer (III)	—	—	—	—	—	100.0	—	—

in the phase transformation from single crystal to amorphous state. The thickness of the amorphous Si layer is mainly determined by the diffusion limit of Si. The amorphousization of single crystal silicon via the doping of other elements has already been reported [22,23]. Sn is not present inside the grains of the annealed sample, which is mainly attributed to the lack of mutual miscibility of Al and Sn. Sn atoms diffuse along the Al grain boundaries to the external surface of the Al film quite easily under thermal activation [24-27].

2.2 Electrical resistivity

The variation of electrical resistivity during annealing was in-situ observed in a 130 nm thick sample, as shown in Fig.2a. The electrical resistivity of the as-deposited film is ~16 μΩ·cm at room temperature and it decreases to ~3.3 μΩ·cm at 703 K. The electrical resistivity is 3.5 μΩ·cm when the sample was heated to 823 K. During the cooling stage of the heating cycle, the electrical resistivity drops almost linearly with the decrease of temperature. The electrical resistivity of the sample at 300 K is found to be ~2.0 μΩ·cm, which is in agreement with the results directly obtained from the annealed sample. The temperature dependence of electrical resistivity is further investigated under cryogenic conditions, which are shown in Fig.2b. The variation of resistivity with temperature is negligible in both as-deposited and annealed samples. However, a slight increment is observed in the 823 K annealed sample. The electrical resistivity of annealed films with a much lowered thickness (~20 nm) was measured to be as low as 0.55 μΩ·cm at 300 K, which is significantly lower than that of 130 nm thick samples. In addition, the electrical resistivity of the annealed 20 nm thick film increases dramatically to 47.76 μΩ·cm when the temperature is lowered to 4 K.

The phenomenon observed in our work is quite abnormal in two aspects. On one hand, the electrical resistivity of thin films is normally much higher than that of the bulk materials due to surface scattering effect of the electronic carriers. The thickness dependence of metallic films resistivity is described by Fuchs-Sondheimer (FS) model [28]:

$$\frac{\rho}{\rho_0} = 1 + \frac{3}{8\kappa}(1-p) \quad \kappa \gg 1 \quad (1)$$

where, ρ₀ and ρ are the resistivities of bulk and film materials, respectively. κ is the ratio between film thickness and the mean electron free path, and p is the fraction of electrons elastically

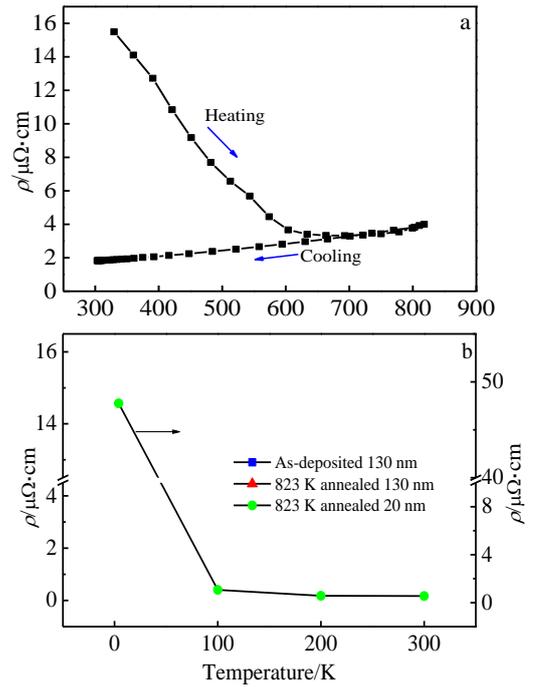


Fig.2 Variation of electrical resistivity as a function of temperature: (a) in-situ observation during annealing and (b) in cryogenic conditions

scattered at the surface. According to the FS model, a resistivity value higher than that of the bulk material can be expected. Even though the electrical resistivity of bulk pure aluminium at 300 K is 2.73 μΩ·cm [29], the electrical resistivity of 100 nm pure Al film is predicted to be about 3.2 μΩ·cm due to surface scattering phenomenon [30], whereas an experimental value of 4 μΩ·cm was reported [11]. The alloying elements tend to result in higher electrical resistivity. When refractory elements such as Ni, Fe and Co are added, their electrical resistivities increase by 4.23 μΩ·cm/at%, 3.47 μΩ·cm/at%, and 2.42 μΩ·cm/at%, respectively, yet further annealing could lead to an even further lowered resistivity of ~5 μΩ·cm [16]. The electrical conductivity of the annealed film reported in this work is much more superior, although a much higher level of doping of alloying elements is added. On the other hand, for metallic materials, the electrical resistivity would decrease when the temperature decreases; the scattering of electrons by photons becomes less severe due to less thermal vibration of the lattice structure. However, the resistivity of a 20 nm sample becomes much higher as the temperature decreases, which will be discussed in the proceeding section.

2.3 Carrier transportation behavior

In order to understand the mechanism of resistivity variation, Hall-effect measurements were carried out to determine the density (η_H) and mobility (μ_H) of electrical carriers, as shown in Fig.3. For the as-deposited sample, both the density and the mobility of carriers remain relatively constant, which is typical

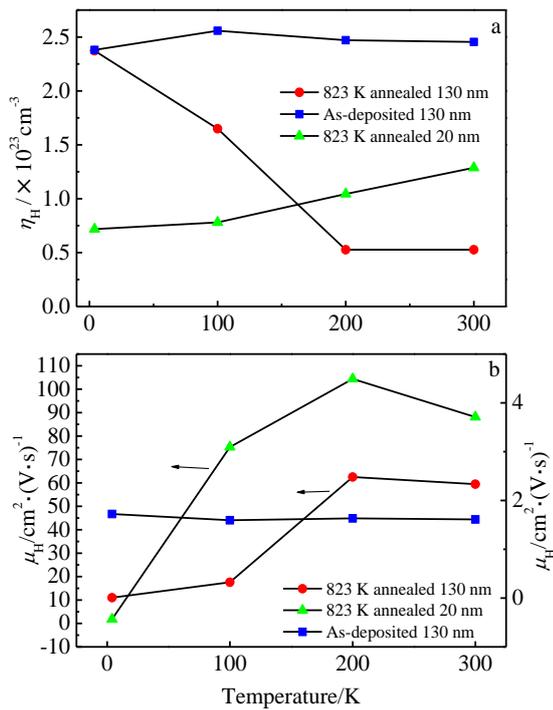


Fig.3 Temperature dependence of density (a) and mobility (b) of Hall carriers for the 130 nm thick as-deposited sample and annealed samples of 130 nm and 20 nm in thickness

behavior of metallic materials. At 300 K, the μ_H value is only $1.61 \text{ cm}^2/(\text{V}\cdot\text{s})$, whereas the η_H is as high as $2.45 \times 10^{23} \text{ cm}^{-3}$. The Hall-effect results of the annealed samples are quite different. The density and mobility of carries were compared for annealed films of different film thicknesses. For the 130 nm thick film samples, the carrier density is $5.27 \times 10^{22} \text{ cm}^{-3}$ at 300 K, which increases dramatically when the temperature decreases ($2.38 \times 10^{23} \text{ cm}^{-3}$ at 4 K). In contrast, the carrier density of the 20 nm thick film sample is $1.29 \times 10^{23} \text{ cm}^{-3}$ and further reduces at cryogenic conditions ($7.18 \times 10^{22} \text{ cm}^{-3}$ at 4 K). For samples of both thicknesses, it is observed that when the temperature decreases, the mobility of Hall-carriers in the annealed samples slightly increases and then falls to a much lower level. In addition, the carrier mobility of the 20 nm thick film sample is higher than that of the 130 nm one.

The Hall-effect measurement results suggest that the low resistivity of the film should be attributed to a combination of high mobility and carrier density in the annealed samples. However, our result shows that the electrical transportation behavior of the 20 nm thick film sample is more similar to that of typical semiconductor materials, even though the carrier density is retained at 10^{22} cm^{-3} to 10^{23} cm^{-3} order of magnitude. For the annealed samples with higher thickness (130 nm), such semiconductor-like behavior is still observable yet much less dominant. The variation of carrier density in the annealed 130 nm thick film could be understood as follows: in Hall measurements, the η_H and μ_H are calculated based upon the

following equations:

$$\eta_H = \frac{1}{|R_H|e} \tag{2}$$

$$\mu_H = \frac{|R_H|}{\rho} \tag{3}$$

where, R_H is the Hall coefficient, and ρ is the resistivity.

Thus, in metal-semiconductor composites, if the temperature increment leads to a higher hole density in the semiconductor via enhanced thermal excitation, the density of Hall carriers can be effectively decreased, as observed in the annealed sample. The variation between the samples of different thicknesses proves that the improved electrical conductivity should be attributed to the underneath interface or substrate. Since the semiconductor-like behavior is not observed in the as-deposited sample, it is more likely that combination of high mobility and carrier density is brought by the film-substrate interface formed during annealing process.

In previous sections, TEM results are actually evidence for the formation of an intimate contact between the substrate and the deposited film. Based on the experimental results, an energy band model is proposed to explain the improved electrical resistivity of the Al alloy film, which is illustrated in Fig.4. For metallic materials (i.e. Al alloy in the present work), the Fermi level of metallic materials is normally high due to its relatively high carrier density. In contrast, the conductivity of semiconductors is relatively low, although a much higher mobility level is normally present. When an intimate contact is formed during the annealing process, the carriers are transmitted to the semiconductor, leading to a much higher carrier density and hence a higher Fermi level. In that case, the Fermi level is demoted into the conducting band of the semiconductor, which might be a reasonable explanation for the improved electrical conductivity of the film. The model we proposed herein is

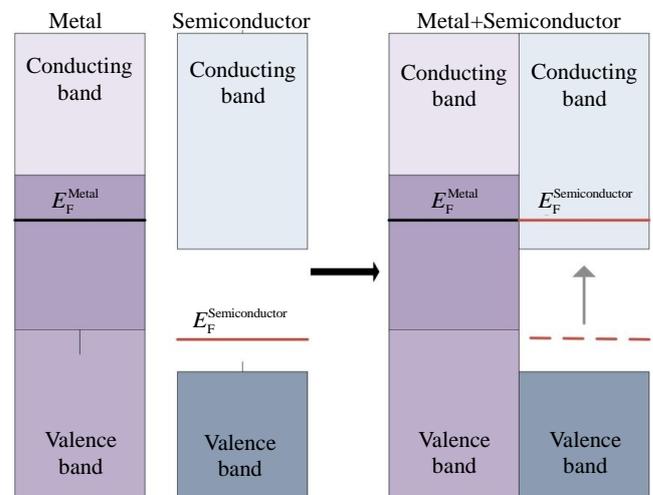


Fig.4 Models proposed to explain the enhanced electronic conductivity by forming an intimate contact with the semiconductor

comparable to what has been established for Ohmic contact between metal and semiconductor materials, conventionally used to deal with the contact resistance between the metal and semiconductor^[31,32]. However, our results demonstrate that a lower in-plane resistivity of the film can also be achieved by forming an intimate contact with the semiconductor.

3 Conclusions

1) By forming intimate contact with the substrate at the interfacial region, a combination of high density and high mobility of carriers can be obtained, which is contributed to the increase of electrical conductivity of the metallic film.

2) The coupled effect should originate from the intimate contact formed between the metallic film and the substrate, which leads to a higher Fermi level in the semiconductor.

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磁控溅射 Al-Fe-Sn 薄膜的电输运性能

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摘要: 在电子工业中, 为了制备低电阻率的Al合金薄膜, 需要对薄膜进行退火。虽然材料的电阻率与其电输运性能密切相关, 然而到目前为止, 对于铝合金薄膜的电输运性能研究甚少。本实验首先利用TEM对于磁控溅射铝合金薄膜的结构, 特别是对其与基底界面处的结构进行了表征。在此基础上, 利用霍尔效应测试了解界面状态的变化对于霍尔载流子浓度及迁移率的影响。结果表明, 在退火过程中, 薄膜与基底之间通过扩散形成紧密接触, 从而使得合金薄膜同时具有较高的载流子浓度以及载流子迁移率。最后, 利用一个新提出的能带模型, 解释所观察到的界面变化对于电导率的影响。

关键词: 电阻率; 铝合金薄膜; 电输运

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